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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/711,167 | 08/30/2004 | Mahmoud A. Mousa | BUR920040020US1 | 5166 |

44152 7590 03/13/2007

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| EXAMINER | |
|---|---|
| CHIU, TSZ K | |
| ART UNIT | PAPER NUMBER |
| 2822 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | NOTIFICATION DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/13/2007 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/13/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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pto@gbpatent.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/711,167 | MOUSA ET AL. | |
| | Examiner | Art Unit | |
| | Tsz K. Chiu | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *14-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claim 14-24 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al. (6821826).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 14, Chan discloses a lower semiconductor device (60, For example Fig. 1c) having an active region comprising a semiconductor with a first crystal orientation (58, For example Fig. 1c); and an upper semiconductor device (20, For example Fig. 1c) having an active region comprising a semiconductor with a second crystal orientation (18, For example Fig.

1c), wherein the upper semiconductor device is formed separately (figure 1b) from the lower semiconductor device and connected thereto by an interconnect structure (75, For example Fig. 1c).

With respect to claim 15, Chan discloses wherein the first crystal orientation is different from the second crystal orientation (Abstract, lines 12-19).

With respect to claim 16, Chan discloses further comprising at least one layer (16, For example Fig. 1c) of a semiconductor device between the lower and upper semiconductor devices.

With respect to claim 17, Chan discloses wherein at least one semiconductor device of the at least one layer of semiconductor device comprises an active region (18, 58, For example Fig. 1c) having a crystal orientation different from the crystal orientation of at least any one of the lower semiconductor device (60, For example Fig. 1c) and the upper semiconductor device (20, For example Fig. 1c).

With respect to claim 18, Chan discloses wherein the upper semiconductor device (20, For example Fig. 1c) is bonded to the top of the lower semiconductor device (60, For example Fig. 1c) with an insulating layer (16, For example Fig. 1c), and wherein at least a portion of the upper semiconductor device (20, For example Fig. 1c) is electrically connected to at least a portion of the lower semiconductor device (60, For example Fig. 1c).

With respect to claim 19, Chan discloses the lower semiconductor device (60, For example Fig. 1c) includes either a pFET device or an nFET device, and the upper semiconductor device (20, For example Fig. 1c) includes either a pFET device or an nFET device; and the crystal orientation of the active region (58, For example Fig. 1c) of the respective lower

semiconductor device is different from the crystal orientation of the active region (18, For example Fig. 1c) of the respective upper semiconductor device.

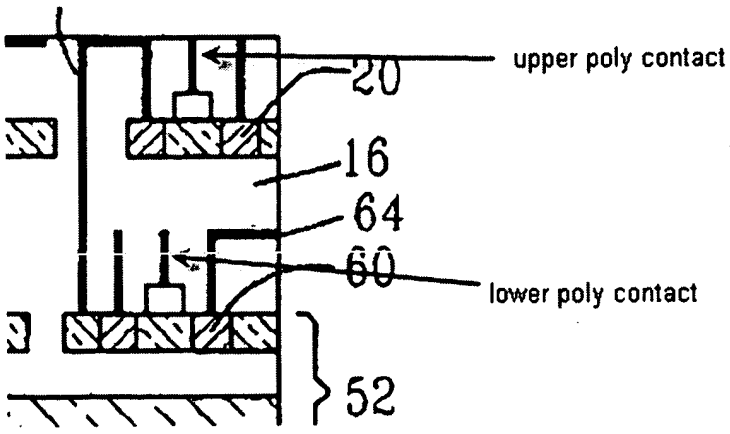
With respect to claim 20, Chan discloses wherein the lower and upper semiconductor devices (20, 60, For example Fig. 1c) comprise an inverter, and the pFET device has a crystal orientation of [100] in an active region and the nFET device has a crystal orientation of [110] in an active region (column 5, lines 11-20).

With respect to claim 21, Chan discloses further comprising a gate oxide (column 5, lines 23-30) formed on a top of the active region of the upper semiconductor device.

With respect to claim 22, Chan discloses further comprising a poly gate (column 5, line 25) formed on a top of the gate oxide, with an upper poly contact to voltage bus (see drawing below).

With respect to claim 23, Chan discloses further comprising metal contacts (24, For example Fig. 1c) connecting to inputs of the upper semiconductor device (20, For example Fig. 1c).

With respect to claim 24, Chan discloses further comprising a lower poly contact (see drawing below) connecting to the voltage bus.



Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TKC
March 4, 2007

Zandra V. Smith
Supervisory Patent Examiner
5 March 2007